a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer.

Please add the following new claims:

--36. The electrical contact of Claim 23 wherein said additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

37. The electrical contact of Claim 36 wherein said additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt or mixtures thereof

38. The electrical contact of Claim 37 wherein said additive is Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or mixtures thereof.

39. The electrical contact of Claim 23 wherein said additive is present in said metal disilicide in an amount of from about 0.01 to about 50 atomic percent.

40. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide having lateral edges, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, said